Q.P. Code: 16EC431 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Supplementary Examinations August-2021

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Explain the steps involved in the fabrication of a n-well process CMOS transistor.	**6M**
	b	Compare CMOS with BJT in different aspects.	**6M**

OR

2	a	Explain the operation of BICMOS inverter with neat diagram.	**6M**
	b	Discuss about (i) Threshold Voltage V_t (ii) Trans-conductance g_m (iii) Output conductance g_{ds}.	**6M**

UNIT-II

3	a	Explain the VLSI design flow.	**8M**
	b	Design the stick diagram for CMOS Inverter.	**4M**

OR

4	a	Explain how PMOS transistor designed using lamda-based design rule.	**7M**
	b	Create the stick diagram for (AB+CD) using NMOS design style.	**5M**

UNIT-III

5	a	Design CMOS implementation of 2x1 MUX using transmission gates.	**6M**
	b	Discuss NORA Logic.	**6M**

OR

6	a	Explain AOI implementation using CMOS design style.	**5M**
	b	Explain clock and power distribution in VLSI Design circuits with neat diagrams.	**7M**

UNIT-IV

7	a	Construct 4*4 array multiplier.	**6M**
	b	Design and Explain 3 bit LFSR with example.	**6M**

OR

8	a	Explain the 6 transistor static memory cell.	**6M**
	b	Design and Explain ripple counter.	**6M**

UNIT-V

9	a	Explain the architecture of FPGA.	**6M**
	b	What is the need for testing? Explain about Fault simulation.	**6M**

OR

10	a	Design the PAL Structure for the Boolean function Y= AB'C'+ABC+A'B'C'+A'BC.	**6M**
	b	Explain stuck at 1 and stuck at 0 faults with neat diagram.	**6M**

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